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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,823	07/10/2003	Jong Hwan Kim	CU-3284 RJS	2689

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LADAS & PARRY
224 SOUTH MICHIGAN AVENUE, SUITE 1200
CHICAGO, IL 60604

EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,823	KIM, JONG HWAN	
	Examiner	Art Unit	
	Luan Thai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/15/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The Information disclosure Statement filed on 8/15/03 has been considered.

Claim Objections

3. Claim **4** is objected to because of the following informalities:

In claim 4, line 4, the recitation "the fourth inter-insulation layer" should be changed to -- a fourth inter-insulation layer—(in case of claim 4 depending on claim 1, which does not recite the fourth inter-insulation layer).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Applicant admitted prior art, Figs. 1A-1D, Specification's pages 1-4 (hereinafter "prior art").

Regarding claim 1, the "prior art" discloses a method for forming bit lines of semiconductor device, comprising the steps of: forming a plurality of word lines (15) and dopant areas on a semiconductor substrate (10) (Fig. 1A); forming first inter-insulation layer (17) on the substrate including the word lines, the first inter-insulation layer including landing plug contacts (18) exposing a part of each dopant area (Fig. 1B); forming landing plugs (19) for embedding the landing plug contacts; forming second and third inter-insulation layers (20-21) in that order on a front surface of the substrate including the landing plugs (19) and forming bit line contacts (22) for exposing the landing plugs by etching of the third and second inter-insulation layers (Fig. 1C); and forming bit lines (23) for embedding the bit line contacts, wherein the word lines each includes a gate insulation layer (12), a gate electrode (13) and a hard mask (14).

6. Claims 1-5 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,251,726).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-5 and 7, Huang discloses a method for forming bit lines of semiconductor device, comprising the steps of: forming a plurality of word lines and dopant areas on a semiconductor substrate (10) (Fig. 1, Col. 5, lines 37+); forming first inter-insulation layer (24) on the substrate including the word lines, the first inter-insulation layer including landing plug contacts exposing a part of each dopant area (Fig.

1); forming landing plugs (26B) for embedding the landing plug contacts; forming second and third inter-insulation layers (28/30) in that order on a front surface of the substrate (10) including the landing plugs (26B) and forming bit line contacts (42) for exposing the landing plugs by etching of the third and second inter-insulation layers (Col. 6, lines 39+); and forming bit lines (44B) for embedding the bit line contacts, wherein the third inter-insulation layer (30) is made of BPSG (Col. 6, lines 45+), the bit lines (44B) are made of metal, and the word lines each includes a gate insulation layer (14), a gate electrode (16) and a hard mask, the gate electrode having a structure of a tungsten silicide layer (Col. 5, lines 32+). Huang further discloses: forming photosensitive layer pattern (Col. 8, lines 22+) on the fourth inter-insulation layer (40), areas for the bit line contacts being defined on the photosensitive layer pattern, forming a fourth inter-insulation layer pattern by etching of the fourth inter-insulation layer using the photosensitive layer pattern as a mask (Col. 8, lines 22+), and forming the bit line contacts for exposing the landing plug contacts by etching of the third and second inter-insulation layers (28/30) using the fourth inter-insulation layer pattern as a mask, wherein the third inter-insulation layer makes use of a silicon-nitride (Col. 6, lines 41+). Since the fourth inter-insulation layer is made of silicon oxide, which is different from BPSG used to form the second inter-insulation layer, their etching ratios are inherently different.

7. Claims 1-2 and 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoo et al. (6,271,125).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-2 and 5-7, Yoo et al. disclose (see specifically figures 1-11) a method for forming bit lines of semiconductor device, comprising the steps of: forming a plurality of word lines (10) and dopant areas on a semiconductor substrate (1) (Fig. 3); forming first inter-insulation layer (19) on the substrate including the word lines (Fig. 6), the first inter-insulation layer including landing plug contacts (21) exposing a part of each dopant area (Fig. 7); forming landing plugs (22a) for embedding the landing plug contacts (Fig. 8); forming second and third inter-insulation layers (23-24) in that order on a front surface of the substrate including the landing plugs and forming bit line contacts (29) for exposing the landing plugs by etching of the third and second inter-insulation layers (Fig. 10); and forming bit lines (33) for embedding the bit line contacts, wherein the word lines each includes a gate insulation layer (3/11), a gate electrode (4/12/13) and a hard mask (9/14/15), the gate electrode having a structure of a tungsten silicide layer (Col. 5, lines52+). Yoo et al. further disclose: the third inter-insulation layer (23) (see Fig. 10) being made of BPSG (Col. 6, lines 49+); the bit line contact holes being formed in a self-align contact mode (Col. 2, lines 59+ and Col. 6, lines 28+); and the bit lines (33) being tungsten structure (Col. 7, lines 35+).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thanhnam/

Luan Thai
United States Patent & Trademark Office
Primary Examiner
Jef-6A15
Art Unit 2827
(571) 272-1935
5/6/04